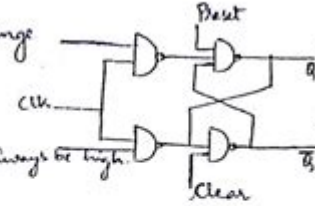


\* In a FF, one opp is always complement of the other.

SR-Flip Flop

	$S_n$	$R_n$	$Q_{n+1}$
Reset	0	0	$Q_n \rightarrow$ No change
Set	0	1	0
	1	0	1
	1	1	x

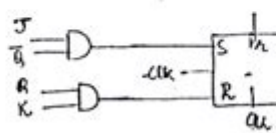


\* During normal operation, preset & clear must always be high.

JK Flip Flop

$J_n$	$K_n$	$Q_{n+1}$
0	0	$Q_n$
0	1	0
1	0	1
1	1	$Q_n'$

When both  $J=K=1 \Rightarrow$  Race around problem occurs.



$\hookrightarrow$  toggling the opp more than once during the clock pulse.

D-Flip Flop

J	K	$Q_{n+1}$
0	1	0
1	0	1

$K = \bar{J}$

- \* Qp same as preset iff.
- \* It provides a delay of one clock pulse.
- \* Used to make transparent latch.
- \* To design a binary counter.

T-Flip Flop

T	$Q_{n+1}$
0	$Q_n$
1	$Q_n'$

$J = K$

It acts as a freq. divider.

- \* The largest binary number that can be represented by an n-bit counter =  $2^n - 1$
- \* Qp signal freq. of Mod-n counter is  $1/n$  of the clk. freq.
- \* # flip flops (n) to construct mod-N counter :  $2^{n-1} \leq N \leq 2^n$ .
- \* # ring counter is N.
- \* # Johnson counter is  $N/2$ .

Binary to gray  $B_2, B_1, B_0 \rightarrow G_2 = B_2, G_1 = B_2 \oplus B_1, G_0 = B_1 \oplus B_0$

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